IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETLIST, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 1:22-cv-00134-LY **JURY TRIAL DEMANDED**
NETLIST, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 1:22-cv-00136-LY **JURY TRIAL DEMANDED**

PLAINTIFF NETLIST, INC.'S SUR-REPLY CLAIM CONSTRUCTION BRIEF REGARDING U.S. PATENT NOS. 8,301,833; 9,824,035; 10,268,608; AND 10,489,314

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Cases

Statutes

I. CLAIM CONSTRUCTION REGARDING THE '833 PATENT

A. Volatile / Non-Volatile Memory Subsystems (Claim 15)

"There are only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning: "1) when a patentee… acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC,* 669 F.3d 1362, 1365 (Fed. Cir. 2012). Neither exception applies here. Netlist's constructions should be adopted.

First, the specification lacks a clear and unmistakable disavowal, and Micron fails to argue one exists. At most, Micron asserts the "specification refers to memory subsystems as distinct from other memory system components." Dkt. 57 ("Reply") at 1. But the portions of the specification Micron relies on are non-limiting embodiments that cannot limit claim scope. *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019) (claim scope cannot be limited based on specification's non-limiting embodiments). Moreover, the specification *does* refer to "other memory system components" as being part of a memory subsystem. Dkt. 55 ("Resp.") at 2; *see, e.g.*, '833 Patent at 18:36-37 ("In one embodiment, for example, *the volatile memory subsystem 30 comprises a 72-bit data bus* . . ." (emphasis added).

Second, the prosecution history lacks clear and unmistakable disavowal. Micron repeats its faulty assertion that Netlist argued in prior IPRs that the disputed "subsystems" of the '833 Patent cannot include a controller. Reply at 1. This is false. In fact, Netlist ***expressly rejected*** that argument during those IPRs. Resp. at 3-4. Moreover, Micron's continued reliance on the Board's statement that, "Petitioner does not explain sufficiently why the controller is a part of the volatile memory subsystem," is misplaced. Reply at 1. As previously noted, that statement is incorrect. Resp. at 3-4. The portion of Netlist's preliminary response the Board cites in support of that statement does not mention a "controller," or that a "controller" cannot be part of a "subsystem."

See Dkt. 41-18 at 56-58. At most, Netlist's statements during prior IPRs are open to multiple reasonable interpretations, and do not amount to a clear and unmistakable disavowal. *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013) (statements amenable to multiple reasonable interpretations cannot be deemed clear and unmistakable).

Third, Micron's argument that, "[m]emory devices can be built with registers included therein" misses the point. Reply at 1. Micron's proposals require "memory devices" to be coextensive with "memory subsystems." But that limited interpretation is inconsistent with plain and ordinary meaning, and contradicted by the specification's teaching that memory subsystems can include more than just memory devices. *See, e.g.*, '833 Patent at 7:8-10 ("the volatile memory subsystem 30 can comprise a registered DIMM subsystem comprising one or more registers 160 and a plurality of DRAM elements 180…"); Fig. 4A ("register 160" is separate from "DRAM elements 180").

Finally, Micron's reliance on dependent claim 16's recitation of a "controller" is misplaced. Reply at 1. Independent Claim 15 is broader than claim 16. Claim 16 recites a "controller" configured to couple and decouple the memory subsystems, but is silent as to whether the "controller" may or may not be part of a memory subsystem. Claim 16 certainly does not recite that all controllers *cannot* be part of a "memory subsystem," and there is no reason to adopt Micron's proposed negative limitation.

B. "controller"[1] (Claim 16)

First, Micron argues that *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311 (Fed. Cir. 2004) is "outdated case law." Micron is wrong. Courts—including the Federal Circuit and this Court—continue to cite to *Linear* for the same proposition as Netlist: "[W]hen the

[1] Full claim terms for all headings are included in the prior briefs.

structure-connoting term . . . is coupled with a description of the [term's] operations, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 ¶ 6 presumptively will not apply." *See, e.g.*, *Dyfan, LLC v. Target Corp.*, No. 2021-1725, 2022 WL 870209, at *6 (Fed. Cir. Mar. 24, 2022); *Sonrai Memory Ltd. v. Oracle Corp.*, No. 1:22-CV-94-LY, 2022 WL 800730, at *9 (W.D. Tex. Mar. 16, 2022).

Micron attempts to distinguish *Linear* by arguing that "the term at issue in *Linear* was 'circuit,' not 'controller . . .'" Reply at 2. Micron misses the point. *Linear* instructs that claim language describing a disputed term's objectives or operations "in sufficient detail" can connote, sufficient structure to avoid § 112(6). 379 F.3d at 1320; *see also Sonrai*, 2022 WL800730, at *8. Micron also attempts to distinguish *Linear* based on its citation to *Apex Inc. v. Raritan Computer, Inc.*, 325, F.3d 1364, 1373 (Fed. Cir. 2003), which "analyzed whether there was also an identifier claim term that connote[d] structure." Reply at 2. But there was no "identifier term" at issue in *Linear*, and the fact that *Apex* may arguably be distinguishable from the instant case on that basis does not mean that *Linear* is similarly distinguishable. Moreover, the Federal Circuit in *Apex* found that "it is clear that the term 'circuit,' by itself connotes some structure"—*i.e.* "circuit" without an "identifier term." *Apex*, 325 F.3d at 1373. Micron's *Apex* argument is a red herring and does not change *Linear's* central premise that § 112(6) may be avoided with sufficient description of "objectives or operations." *Linear*, 379 F.3d at 1320.

Second, Micron's argument that "controller" is inherently a nonce word also fails. Reply at 2. Micron does not address, much less rebut, Netlist's four cited authorities holding "controller" is ***not*** a nonce word. *See* Resp. at 6. Netlist, on the other hand, has distinguished the case on which Micron relies, *Incom Corp. v Radiant RFID, LLC*, No. 1-17-cv-0009-LY, 2018 WL 4690934 (W.D. Tex. Sep. 28, 2018). *Id*.

Third, Micron argues that Netlist's arguments fail to take this term "outside the bounds of § 112(6)." Reply at 3. But Micron has the burdens reversed. *Sonrai*, 2022 WL 800730, at *8 ("Defendant bears the burden of overcoming the presumption that § 112, ¶ 6 does not a apply by a preponderance of the evidence."). Critically, Micron fails to proffer any evidence to justify the application of § 112(6). Micron merely asserts, in a conclusory manner, that Netlist's arguments are wrong. Micron fails to (1) rebut Netlist's citations, (2) explain why the specification supports its position, or (3) rebut the testimony of Netlist's expert that a POSITA would have understood the claimed "controller" belongs to a known class of memory technology components. *See* Resp. at 5; Przybylski Decl. at ¶ 40; *see also*, *VDPP LLC v. VIZIO, Inc*., 2021-2040, 2022 WL 885771, at *3 (Fed. Cir. Mar. 25, 2022) (holding it improper to overlook intrinsic evidence in the specification showing that "processor" and "storage" connote structure to a skilled artisan). Thus, Micron fails to carry its burden of showing that § 112(6) applies here.

Finally, Micron asserts that, "Netlist argues that a controller is considered part of the . . . subsystems." Reply at 3. Again, Micron mischaracterizes Netlist's position. Netlist is not arguing that a controller *must be* part of the subsystems. Rather, Netlist's position is that "volatile and non-volatile memory subsystems *may or may not include* certain types of control elements." Resp. at 7 (emphasis added).

II. CLAIM CONSTRUCTION REGARDING THE '035 AND '608 PATENTS

A. "module control device" ('035 and '608 Patents, Claim 1)

Micron does not address the substance of Netlist's arguments that make clear the claimed "module control device" is not subject to § 112(6). As explained above, Micron is wrong that *Linear Tech.* is no longer applicable. *See supra* Section I.B.

Micron fails to contend with Dr. Przybylski's testimony that a POSITA would understand the claims require a "module control device" with connections to signal traces for receiving

commands from a memory controller, and connections to command signal traces coupling the module control device to other memory module components. *See* Przybylski Decl., ¶ 56.[2] Nor does Micron address Dr. Przybylski's testimony that a POSITA would understand the scope of the claim excludes certain control structures and implementations of the "module control device." *See id.* at 8-9. Micron cannot tenably assert that the claims "provide no detail as to how a module control device is implemented." Reply at 4. Netlist identified the detail; Micron and its expert ignored it.

Moreover, Micron relies on *MTD Prods. Inc. v. Inacu,* 933 F.3d 1336 (Fed. Cir. 2019) to summarily dismiss the specification's disclosure of structure. Reply at 5. But *MTD* merely instructs courts to refrain from relying *solely* on the specification to impart structure to nonce terms; the specification is always relevant to a § 112(6) inquiry. *See MTD*, 933 F.3d at 1344; *see also Inventio AG v. ThyssenKrupp Elevator Americas Corp.*, 649 F.3d 1350, 1357 (Fed. Cir. 2011) ("It is proper to consult the intrinsic record, including the written description," in a § 112(6) analysis). Micron concedes that the specification describes "how the inputs of the 'module control device' are coupled to lines and its location," but wrongly suggests that this description does not convey the "internal structure" of the "module control device." Reply at 5. Micron sets the bar higher than the Federal Circuit requires: "[s]tructure may [] be provided by

[2] Regarding how the claimed "module control device" interacts with other components, Micron first contended that the claim language provides "little, if any" detail regarding how the "module control device" interacts with other claimed components. Dkt. 41 ("Op. Br.") at 11. Netlist responded, pointing out that the claims describe with specificity that the claimed "module control device" must "receive memory command signals *from the memory controller via control/address signal lines* . . . [and] recite that the 'module control device' outputs module command signals and module control signals *to memory devices and buffer circuits*, respectively." Resp. at 9 (emphasis in original). Now, unable to credibly argue that the interconnections are not identified, Micron argues—without any support—that they do not provide structure. Reply at 4. They do. *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1351 (Fed. Cir. 2015).

describing the claim limitation's operation, such as its input, output, or connections." *Sonrai*, 2022 WL 800730 at *9 (citing *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1299 (Fed. Cir. 2014)). Micron is also wrong that such description does not reflect the module control device's inner structure. Netlist explained why it does. *See* Resp. at 10-11. Micron cannot dodge the result compelled by the claim language, controlling case law, and specification by avoiding them.

B. "logic" ('035 Patent, Claim 1)

Micron cannot transform the claimed "logic" into a "black box recitation of structure" merely by calling it one. Reply at 6. Again, Micron ignores unfavorable case law by contending that Netlist's *six cited cases* are inapplicable because they post-date *Williamson* or otherwise rely on outdated authority. This is wrong. *See supra* Section I.B.

In *Sonrai*, this Court analyzed two "logic" terms in the context of § 112(6), rejecting arguments similar to Micron's. 2022 WL 800730, at *6-11. The *Sonrai* defendant argued (as does Micron) that (1) "logic" is a nonce word that does not connote sufficiently definite structure, (2) *Egenera* compels that "logic" is a nonce term, and (3) the specification did not connote a particular structure or class of structures to a POSITA. *Id.* at 8-10. This Court disagreed, holding that "logic" is not subject to § 112(6) if the "stated objectives and operation of the logic connote sufficiently definite structure." *Id.* at 8 (citing *Linear*, 379 F.3d at 1320). This Court also held that § 112(6) did not apply because "[t]he claims themselves connote sufficient structure by describing how the 'logic for' terms operate within the claimed invention to achieve their objectives." *Id.* at 9. Regarding *Egenera*, this Court stated that "the Federal Circuit did not generally hold [in that case] that the term 'logic' is a generic substitute for 'means.'" *Id.*[3]

[3] Netlist explained that the *Egenera* court drew a distinction between logic claimed as "circuitry"—which does convey sufficient structure—and logic claimed as an abstract concept referring to computer operations generally, which does not. Resp at 13. Micron ignores this distinction.

Here, Netlist has shown that the claims connote sufficient structure by describing how the claimed "logic" operates within the claimed invention to achieve its objective. *See Sonrai*, 2022 WL 800730, at *8. Dr. Przybylski explained that a POSITA would understand the claimed "logic" includes logic circuitry to obtain timing information and control circuitry to control the timing of signals on the data path, as well as a decoder to interpret the module control signal. *See* Resp at 14 (citing Przybylski Decl. at ¶ 71).[4] Micron (again) completely ignores Dr. Przybylski's testimony and does not attempt to analyze, rebut, or even address it.

Micron waves away the specification's extensive disclosure of the claimed "logic"—detailed in Netlist's Response and expert declaration—arguing it is irrelevant to the Court's analysis. Reply at 7. But any analysis under § 112(6) must be conducted "in light of the specification." *Sonrai*, 2022 WL 800730, at *10. Micron's failure to address the specification's disclosure of the claimed "logic" provides an independent basis to reject Micron's arguments.

Micron points to purported contradictions between the "logic" claimed in the '035 and '314 Patents as evidence that the term has no specific structure.[5] Reply at 6-7. But, importantly, this *underscores*—rather than undercuts—Netlist's arguments. The context provided by the claims and specification in the '035 Patent make clear to a POSITA that the claimed "logic" refers to *particular* control, data, and timing circuitry configured to respond to *particular* signals generated from *particular* structural components, obtain timing information during *particular*

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[4] Dr. Przybylski also explained why certain logic structures and implementations would fall outside the scope of the claims. *Id.* at 14-15.

[5] Micron also states that the specification's reference to "logic circuit" would render "logic" superfluous if it means "circuit." Reply at 6. But Netlist has not argued that "logic" literally means "circuit." Instead, a POSITA looking at the claims would understand "logic" as being circuitry capable of performing logic functions, and that implementations of the claimed "logic" that are not circuitry capable of performing logic functions are excluded. *See* Resp at 14-15 (citing Przybylski Decl. at ¶ 72).

operations, and control timing of *particular* signals traveling along a *particular* data path. *See* Resp. at 13-14 (citing Przybylski Decl. at ¶¶ 69-72).[6] The particularity with which a POSITA would understand the terms in light of the intrinsic record reflects the structure conveyed by the claims.

C. "command processing circuit" ('608 Patent, Claim 1)

In the face of *sixteen cases* where courts have found "circuit" terms to convey structural meaning, Micron deflects by asserting they are all irrelevant, "outdated" authority. Reply at 8. Micron's position appears to be that nearly two decades of case law from courts across the nation analyzing the word "circuit" should be disregarded following *Williamson*. The Eastern District of Texas recently and squarely addressed this issue, finding that "this line of precedent . . . cannot simply be swept aside by invoking *Williamson*." *Estech Sys., Inc. v. Burnco Texas LLC*, No. 2:20-CV-00275, 2021 WL 2530959, at *17 (E.D. Tex. June 18, 2021). The Federal Circuit cited to *Apex* as recently as *two weeks ago* for the proposition that "'circuit,' by itself connotes some structure." *See Dyfan*, 2022 WL 870209, at *4 (citing *Apex*, 325 F.3d 1364, 1373 (Fed. Cir. 2003)); *see also Ma. Inst. of Tech. v. Abacus,* 462 F.3d 1344, 1355-56 (Fed. Cir. 2006) (finding the recitation of "aesthetic correction circuitry" sufficient to avoid § 112(6) treatment because the term circuit, combined with a description of the function of the circuit, connoted sufficient structure to one of ordinary skill in the art); *see also Linear*, 379 F.3d at 1319-21 (finding that "circuit [for performing a function]" was sufficiently definite structure because the claim recited the "objectives and operations" of the circuit). *Micron*'s single cited case analyzing "circuit" itself quotes *Apex*, albeit selectively.[7]

[6] Again, Micron's Reply leaves Dr. Przybylski's testimony on this unrebutted and unaddressed.
[7] *See Limestone Memory Sys. LLC v. Micron Tech., Inc.*, No. 8:15-CV-00278, 2019 WL 6655273, at *18 (C.D. Cal. Sept. 11, 2019).

Because the Federal Circuit has found that the term "circuit" ***by itself*** connotes some structure, "'the presumption that § 112(6) does not apply is determinative' in the absence of 'more compelling evidence of the understanding of one of ordinary skill in the art.'" *Dyfan*, 2022 WL 870209, at *4. *Limestone*, cited by Micron, does not compel a different analysis.[8]

In its Response, Netlist enumerates the numerous functions attributable to the "command processing circuit" and identifies with particularity how the function and operation of the claimed "command processing circuit" convey inherent structure to a POSITA. Resp. at 17-18. Micron's expert does not respond to or rebut this analysis, and Micron does not dispute that a POSITA would understand that this structure is conveyed by the claim language; instead, Micron vaguely insists that more is required. Reply at 8. This is wrong. *See, e.g., Linear Tech.,* 379 F.3d at 1320 ("[W]hen the structure-connoting term 'circuit' is coupled with a description of the circuit's operation…§ 112 ¶ 6 presumptively will not apply.").

Netlist also described the specification's discussion of the structure and operation of the "command processing circuit." Resp. at 18. Micron does not explain why Netlist's cited passages do not link function to structure, or why the details regarding how the "command processing circuit" interacts with other components does not convey structure to a POSITA. Reply at 9. In sum, Micron fails to offer the kind of "compelling evidence" required to rebut the presumption that § 112(6) does not apply. *See Dyfan*, 2022 WL 870209, at *4 (citing *Apex*, 325 F.3d at 1373).

[8] *Limestone* is inapplicable because there the undisputed evidence was that the plain and ordinary meaning of "activation control circuit" was exceedingly broad. 2019 WL 6655273, at *19. Moreover, *Limestone* reflects a minority view that "logical" descriptions of the functions performed by a claimed circuit cannot convey sufficient structure. *Id.* at *19 ("Thus, logical, functional descriptions of a claim limitation are not a substitute for corresponding structure."). This holding is inconsistent with *Apex* and its progeny. *See Abacus,* 462 F.3d at 1355 (Fed. Cir. 2006) ("[T]he term 'circuit,' combined with a description of the function of the circuit, connote[] sufficient structure to one of ordinary skill in the art to avoid 112 ¶ 6 treatment."); *see also Linear*, 379 F.3d at 1320.

III. CLAIM CONSTRUCTION REGARDING THE '314 PATENT

A. "burst of data strobes" (Claims 1, 15, 25, and 28)

Micron argues that this "term is indefinite because it is susceptible to multiple different interpretations." Reply at 9. But the test of indefiniteness is whether the claims inform a POSITA about the scope of the invention with reasonable certainty. *Nautilus, Inc. v. Biosig Inst., Inc*., 572 U.S. 898, 910 (2014). "The test is not merely whether a claim is susceptible to different interpretations." *Nevro Corp. v. Boston Scientific Corp*., 955 F.3d 35, 41 (Fed. Cir. 2020). Indeed, the Supreme Court declined to adopt such a rule in *Nautilus*. *Id*. (citing *Nautilus*, 572 U.S. at 909).

Moreover, this term is not susceptible to multiple meanings. At most, this term—having the ***same*** meaning—can be applied to *different contexts*. But that is insufficient to invalidate the claims for indefiniteness. *Dyfan,* 2022 WL 870209, at *4 ("Claim terms 'need not connote a single, specific structure,' and may instead 'describe a class of structures' and still recite 'sufficiently definite structure' to not invoke § 112(6).") (quoting *Apple*, 757 F.3d at 1300). Micron fails to present any evidence—much less clear and convincing evidence—to compel a different conclusion. *BASF Corp. v. Johnson Matthey Inc*., 875 F.3d 1360, 1365 (Fed. Cir. 2017) ("[Defendant] had the burden of proving indefiniteness by clear and convincing evidence.").

Notably, Micron now admits that examples of "bursts of data strobes can be found in the figures of the '314 Patent." Reply at 10. A POSITA would also know that examples of related bursts of data signals are found in the '314 Patent's figures. *See, e.g.*, '314 Patent at Figure 6A. Micron further concedes that the term "burst of N-bit wide data signals" has a clear meaning. *Id*. at 9, n.1. It is therefore inconceivable that a POSITA understanding data *signals* can be grouped together in bursts would not also understand data *strobes* can be grouped together in related bursts—particularly when the specification provides clear examples.

Finally, Micron's continued reliance on *Dow* and *Teva* is unavailing. In *Dow*, the term at issue was "a slope of strain hardened coefficient greater than or equal to 1.3." *Dow Chem. Co. v. Nova Chemicals Corp. (Canada)*, 803 F.3d 620, 634-35 (Fed. Cir. 2015). In that case, there was no established way to calculate the claimed slope and, as a result, the patent owner's expert resorted to fabricating his own method of calculating the slope that was not disclosed in the intrinsic record. *Id*. In *Teva*, the limitation at issue was "molecular weight of about 5 to 9 kilodaltons." *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1338 (Fed. Cir. 2015). There, the specification failed to address the fact that that "molecular weight" could be calculated in different ways. *Id*. at 1344-45. The Federal Circuit concluded in both cases that the disputed terms were indefinite based on the existence of multiple ways of calculating the critical claim elements. *Id*.; *Dow*, 803 F.3d at 635. Here, infringement does not turn on any precise calculations, and the intrinsic record includes relevant teachings regarding the meaning of "burst of data strobes."

B. The "Logic" Terms (Claims 1, 15, and 25)

Micron falls short of satisfying its burden to show that § 112(6) applies for the same reasons set forth above for Netlist's other patents. *See supra* Section II.B. In addition, using claim 1 of the '314 Patent as an example, Micron argues that the § 112(6) analysis for the claimed "logic" must be limited to the phrase "logic coupled to the circuitry and configured to respond to the first memory command," and cannot include a consideration of the "other" claimed functionalities of the claimed logic (*e.g.,* receiving, decoding, generating, communicating). Reply at 12. Micron then uses its own narrow reading of claim 1 to distinguish cases like *Rodime PLC v. Seagate Tech., Inc.*, 174 F.3d 1294 (Fed. Cir. 1999), arguing that a claimed physical connection between the "logic" and another component is "not enough" to avoid § 112(6). Micron's argument is fundamentally flawed.

Section 112(6) determinations must be made under the traditional claim construction principles in light of the claims ***as a whole***. *Dyfan,* 2022 WL 870209, at *6. A § 112(6) analysis that removes a claim term from its context, which otherwise strongly suggests the plain and ordinary meaning of the term, is erroneous. *Zeroclick, LLC v. Apple Inc*., 891 F.3d 1003, 1008 (Fed. Cir. 2018) (district court's analysis removing the claim terms from their context was erroneous); *see also Dyfan*, 2022 WL 870209, at *6-8 (disputed terms did not invoke § 112(6) based on claims and surrounding context). Micron limits its analysis to a "specific" logic functionality, deliberately ignoring other claimed functionalities and capabilities relating to "logic" that a POSITA would look to for guidance. *See* Resp. at 24-25; Przybylski Decl., §112. Micron's failure to consider the claims ***as a whole*** dooms its position here. *See, e.g*., *Sonrai*, 2022 WL 800730, at *9 (finding that the context in which the term "logic" is used in the claims and specification provides sufficient structural meaning to a POSITA).

Micron also argues that an analysis of the specification is irrelevant to the initial inquiry as to whether § 112(6) applies. Reply at 11. Micron is wrong again. The § 112(6) analysis must "naturally look to the specification, prosecution history, and relevant external evidence to construe" potential § 112(6) limitations. *Apple*, 757 F3d at 1296; *see also VDPP*, 2022 WL 885771, at *3 (holding that the district court improperly overlooked intrinsic evidence in the specification showing that the terms "processor" and "storage" connote structure to a skilled artisan); *Zeroclick*, 891 F.3d at 1008-9 (finding that § 112(6) did not apply based, in part, on an analysis of the specification); *Sonrai*, 2022 WL 800730, at *10 ("The specification further confirms that the 'logic for' terms do no invoke § 112(6)."). Here, the specification supports Netlist's position that § 112(6) does not apply. Resp. at 23-24; Przybylski Decl., § 113-115; *see also Dyfan*, 2022 WL 870209, at *4 ("Claim terms 'need not connote a single, specific

structure," and may instead "describe a class of structures" and still recite 'sufficiently definite structure' to not invoke § 112(6).") (quoting *Apple*, 757 F.3d at 1300). Indeed, the specification not only identifies the relevant structures, but even instructs the reader where to buy those structures. *See, e.g.*, '314 Patent at 7:5-19. Thus, there can be no reasonable dispute that the structures existed in the prior art at the time of the invention. *VDPP*, 2022 WL 885771, at *3 (quoting *Zeroclick*, 891 F.3d at 1008).

Significantly, Micron fails to cite any evidence from the specification that would support its own § 112(6) argument. Instead, Micron simply argues—in a conclusory manner—that the '314 Patent specification lacks any relevant disclosures, and that § 112(6) should apply based on Netlist's alleged failure to sufficiently link the specification's disclosures and the claimed "logic." Micron's arguments miss the mark again. It is Micron's burden to show that § 112(6) applies, a burden Micron cannot carry by ignoring the specification and the claims as a whole. *See Zeroclick*, 891 F.3d at 1008-09 (rejecting Apple's argument that § 112(6) applied because it provided no evidentiary support for that position).

C. "overall CAS latency . . ." / "actual operational CAS latency" ('314 Patent: Claims 1, 15, 25, 28)

The plain and ordinary meaning must apply unless a patentee acts as his own lexicographer or when there is a clear and unmistakable disavowal. *Sonrai*, 2022 WL 800730, at *4. Here, Micron fails to even argue that the patentee acted as his own lexicographer, or disavowed claim scope. The parties also largely agree that, to a POSITA, the meaning of CAS latency generally relates to a delay between the time when a command is sampled (or executed) and the time when the first piece of data is available. Thus, the Court should adopt the plain and ordinary meanings of the CAS latency terms, and reject Micron's proposal to exclude write commands from that delay. That approach would resolve the parties' dispute here. *See Finjan,*

Inc. v. Secure Computing Corp., 626 F.3d 1197, 1207 (Fed. Cir. 2010) (holding that the district court did not err by adopting a term's plain and ordinary meaning while rejecting the defendant's proposed construction, which resolved the parties' quarrel). Alternatively, the Court should adopt Netlist's proposed construction which takes into consideration both read and write commands.

Micron now disingenuously argues that its proposals "do[] not exclude write commands." Reply at 13. That is misleading. Micron's proposed construction of "overall CAS latency of the memory module" is specifically tied to "the time when a ***read*** command is executed . . ." The same applies to the other term. Thus, according to Micron's narrowing language, the limitations cannot be satisfied when a ***write*** command is executed. Micron's attempt to limit the CAS latency terms to just read commands is flawed and contradicted by the intrinsic evidence as explained previously. Resp. at 26-28. Critically, Micron failed to identify any disavowal of claim scope, or rely on the intrinsic evidence at all, in its attempt to limit claim scope here. Micron's proposals should therefore be rejected. *See Sonrai*, 2022 WL 800730, at *4.

Further, Micron asserts that Netlist's proposed alternative constructions remove the concept of latency from the claim terms. Not so. Netlist's proposed alternative constructions describe how a POSITA would determine the relevant CAS latencies. Since Netlist specifically addresses how to determine the CAS latencies, it has not "removed" them as a concept. Micron also claims that that the start and stop times included in Netlist's proposals will always be the same for write commands. But Micron's (incorrect) argument lacks any evidentiary support. Even assuming, *arguendo*, that Micron is correct (it is not), that just means that the latency values will be zero, which does not amount to removing the concept of latency from the claims.

D. The "Circuitry" Terms (Claims 1, 15, 25, 28)

Micron fails to satisfy its burden to show that § 112(6) applies for the same reasons set forth above for Netlist's other patents. *See supra* Section II.C. Further, Micron argues that the

claim language does not impart sufficiently definite structure into the term "circuitry" and, therefore, "does not disqualify" the claim from § 112(6) treatment. Reply at 14. However, it is not Netlist's burden to "disqualify" this claim term from § 112(6) treatment; it is Micron's burden to overcome the presumption against application of § 112(6), and affirmatively establish that § 112(6) applies. *Sonrai*, 2022 WL 800730, at *8. Critically, Micron failed to provide its own detailed analysis of the claims as a whole to satisfy its burden. Micron also failed to rebut the fact that, when viewed in the context of the claims as a whole, the claimed "circuitry" is a specific type of circuitry that is capable of multiple different functions and operations. Resp. at 29-30; Przybylski Decl., ¶¶ 146-150. Micron's failure to consider the claims as a whole is fatal given its burden to establish that § 112(6) applies.[9]

Micron also argues that Netlist's "citations to the specification cannot salvage its argument." Reply at 14. But again, it is Micron's burden to evaluate the intrinsic evidence to show that § 112(6) should apply. And here, Micron failed to perform that detailed analysis. In fact, Micron's Reply includes no citations to the intrinsic record at all. Instead, Micron relies on its own expert's conclusory opinion that the claimed "circuitry" allegedly "has no corresponding structure." Reply at 15. But those types of (extrinsic) conclusory opinions from an expert carry no weight. *See Phillips v. AWH Corp*., 415 F.3d 1303, 1318 (Fed. Cir. 2005). Overall, Micron cannot carry its burden by ignoring the specification and claims as a whole. *Zeroclick*, 891 F.3d at 1008-09. The Court should find that § 112(6) does not apply here.

[9] Micron failed to distinguish cases like *Inventio*, *Abacus*, *Linear*, *Apex*, and *Rodime* for the reasons set forth above. *See supra* Sections I.B, II.A, II.C.

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CERTIFICATE OF SERVICE

I hereby certify that on April 7, 2022, counsel of record who are deemed to have consented to electronic services are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(b)(1).

/s/ *Rex Hwang*